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THESIS FOR THE DEGREE OF LICENTIATE OF ENGINEERING

InP High Electron Mobility Transistor Design for Cryogenic Low Noise Amplifiers

EUNJUNG CHA

Microwave Electronics Laboratory
Microtechnology and Nanoscience - MC2
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2018

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ISSN 1652-0769
Technical Report MC2-387

Cover:
Cross sectional STEM image of the InP HEMT

Printed by Chalmers Reproservice
Gothenburg, Sweden March 2018

Abstract

The InGaAs/InAlAs/InP high electron mobility transistor (InP HEMT) is the superior technology for the most demanding low-noise and high-speed microwave and millimeter-wave applications, in particular in radio astronomy and deep-space communication. InP HEMT has enabled cryogenic low noise amplifier (LNA) designs with noise temperatures about ten times the quantum noise limit from sub GHz up to 120 GHz. In this thesis, design techniques of 100 nm gate length InP HEMTs for state-of-the-art cryogenic LNAs are reported. Detailed DC, RF and noise analysis for the InP HEMTs at 300 K and 5 K are presented. The thesis is divided into two parts.

The first part of the work reports on the optimization of 100 nm gate length InP HEMT technology for cryogenic LNA applications at microwave frequencies. By scaling the gate length and barrier thickness combined with reduction of source and gate resistances, advances in cryogenic noise performance for wideband monolithic microwave integrated circuit (MMIC) LNA were demonstrated in the frequency range 0.3−28 GHz. At 4 K, the minimum noise temperature was 2.2 K and 4.8 K for a 0.3−14 GHz and 16−28 GHz LNA, respectively. The cryogenic MMIC LNAs demonstrated state-of-the-art noise performance.

In the second part, cryogenic stability of two-finger InP HEMTs is investigated. The InP HEMTs exhibited anomalous behavior in terms of jumps in drain current, sharp peaks in transconductance, and decreased gain under cryogenic operation. Three different design techniques for two-finger HEMTs were tested to mitigate the anomalous instabilities associated with cryogenic operation. By either adding a source air-bridge, connecting the back end of gates or increasing the gate resistance, stable device operation was demonstrated for each case. Successful stabilization was confirmed both on device and circuit level by cryogenic measurements. A three-stage 24–40 GHz and a four-stage 28–52 GHz MMIC LNA based on the source air-bridge design technique for the two-finger InP HEMTs were demonstrated at 5.5 K. The minimum noise temperature was 7 K and 6.7 K in the 24−40 GHz and 28−52 GHz LNA, respectively. Both designs demonstrated the lowest noise temperature reported so far for cryogenic MMIC LNAs for these frequency bands.

Keywords: cryogenic, InP HEMT, LNA, MMIC, noise temperature, stability.

List of publications

Appended papers

This thesis consists of an extended summary and the following appended papers:

[A] **Eunjung Cha**, Giuseppe Moschetti, Niklas Wadefalk, Per-Åke Nilsson, Stella Bevilacqua, Arsalan Pourkabirian, Piotr Starski, and Jan Grahn,"Two-Finger InP HEMT Design for Stable Cryogenic Operation of Ultra-Low-Noise Ka- and Q-Band LNAs", IEEE Transactions on Microwave Theory and Techniques, vol. 65, no. 12, pp. 5171-5180, Dec 2017. DOI: 10.1109/TMTT.2017.2765318

[B] **Eunjung Cha**, Niklas Wadefalk, Per-Åke Nilsson, Joel Schleeh, Giuseppe Moschetti, Arsalan Pourkabirian, Silvia Tuzi, and Jan Grahn,"0.3−14- and 16−28-GHz Wide-Bandwidth Cryogenic MMIC Low-Noise Amplifiers", submitted, 2017.

[C] **Eunjung Cha**, Arsalan Pourkabirian, Joel Schleeh, Niklas Wadefalk, Giuseppe Moschetti, Piotr Starski, Göran Alestig, John Halonen, Bengt Nilsson, Per-Åke Nilsson, and Jan Grahn,"Cryogenic low-noise InP HEMTs: A source-drain distance study", in International Conference on Indium Phosphide and Related Materials (IPRM), Toyama, Japan, 2016.

Other papers and publications

The following papers and publications are not appended to the thesis, either due to contents overlapping with appended papers, or due to contents not related to the thesis.

[a] **Eunjung Cha**, Giuseppe Moschetti, Niklas Wadefalk, Per-Åke Nilsson,

Stella Bevilacqua, Arsalan Pourkabirian, Piotr Starski, and Jan Grahn, "Two-Finger InP HEMT Design for Stable Cryogenic Operation of Ultra-Low-Noise Ka-Band LNAs", in 2017 IEEE MTT-S International Microwave Symposium (IMS), Honolulu, Hawaii, 2017.

[b] Joel Schleeh, Giuseppe Moschetti, Niklas Wadefalk, **Eunjung Cha**, Arsalan Pourkabirian, Göran Alestig, John Halonen, Bengt Nilsson, Per-Åke Nilsson, and Jan Grahn, "Cryogenic LNAs for SKA band 2 to 5", in 2017 IEEE MTT-S International Microwave Symposium (IMS), Honolulu, Hawaii, 2017.

[c] Yulung Tang, Niklas Wadefalk, Jacob W Kooi, Joel Schleeh, Giuseppe Moschetti, Per-Åke Nilsson, Arsalan Pourkabirian, **Eunjung Cha**, Silvia Tuzi, and Jan Grahn, "Cryogenic W-band LNA for ALMA band 2+3 with average noise temperature of 24 K" in 2017 IEEE MTT-S International Microwave Symposium (IMS), Honolulu, Hawaii, 2017.

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Chapter 1

Introduction

Since the invention of the high electron mobility transistor by T. Mimura in 1979,[1] HEMTs have been the superior technology in the most demanding low-noise and high-speed microwave and millimeter-wave applications, in particular for radio astronomy and deep-space communication. In the HEMT heterostructure, the electrons are confined in the channel forming the two-dimensional electron gas where the impurity scattering with ionized donors is suppressed. As a results, an electron mobility becomes more than ten times higher than in silicon at a comparable sheet charge density meaning extremely high-frequency and low-noise properties for the HEMT. The HEMT technology has shown marked improvement with cut-off frequency (f_T) in excess of 600 GHz and maximum oscillation frequency (f_{max}) exceeding 1 THz.[2–7]

One of the great challenges in radio astronomy and deep-space communication is to detect extremely weak signals.[8] For a given antenna, the microwave frontend controls the receiving system sensitivity (S) where S is the quotient $S = G/T_{sys}$ between the antenna gain (G) and the noise temperature (T_{sys}) of the entire receiving chain. Thus improved receiving performance can be achieved by either increasing G or reducing T_{sys}, or both. It is more efficient and cost effective to decrease T_{sys}, in particular by improving the LNA in the first stages of the receiver system, than to improve G which is related to the antenna size and geometry. The noise temperature of the LNA is crucial for T_{sys}. As a result, such an LNA is normally operated at cryogenic temperature, typically 5−15 K. The transistor technology used for the cryogenic LNA design is here decisive for the noise temperature.

The InGaAs/InAlAs/InP HEMT enables the design of cryogenic LNAs with noise temperatures about ten times the quantum noise limit from sub GHz up to 120 GHz.[9–16] Further noise improvement is desirable since a small reduction in noise temperature means higher data reception capability. In addition, pushing the ultra-low noise HEMT technology is also important for research related to quantum physics, such as readout of qubits in quantum computing applications.

The goal of this thesis is to present design techniques for 100 nm gate length InP HEMTs for new state-of-the-art cryogenic LNA up to 50 GHz. Scaling of the gate length and the barrier thickness combined with reduction of source and gate resistances of the InP HEMT have been carried out with respect to noise performance in the cryogenic LNA. Furthermore, design techniques of the two-finger HEMTs for stable cryogenic operation are reported. The cryogenic instability observed in two-finger InP HEMTs is discussed and stabilization

solutions are presented. The stabilized InP HEMTs were implemented in 24−40 GHz and 28−52 GHz cryogenic MMIC LNAs, resulting in state-of-the-art noise performance.

In Chapter 2, the InP HEMT scaling optimized for cryogenic LNA application is discussed. Chapter 3 presents the two-finger HEMT design techniques for stable cryogenic operation. Finally, Chapter 4 summarizes the results of this thesis and provides a future outlook.

Chapter 2

InP HEMT scaling for cryogenic LNAs

In order to predict the minimum noise temperature (T_{min}) of the HEMT, an empirical expression suggested by M. Pospieszalski[17] is widely used:

$$T_{min} \approx 2\frac{f}{f_T}\sqrt{(R_s + R_g + R_i)T_g G_{ds} T_d} \tag{2.1}$$

where R_s, R_g, and R_i are the source, gate, and intrinsic channel resistances, respectively. G_{ds} is the output conductance, T_g is the equivalent temperature of R_i, and T_d is the equivalent temperature of G_{ds}. One way of improving the noise performance of HEMT is to maximize the intrinsic f_T and to minimize the parasitic source and gate resistances. However, an aggressive scaling of the Schottky barrier thickness of the HEMT for highest possible f_T will end up increasing the gate leakage current and gate-to-channel capacitance which in turn deteriorate the low-noise performance.[10, 17–19] A thin barrier will also increase the channel depletion and thus the intrinsic resistance due to surface states being closer to the channel.[20] Therefore, a well-balanced vertical and lateral scaling of the HEMTs is required in order to improve the noise performance of the cryogenic LNA.

This chapter addresses an optimized InP HEMT design for cryogenic LNA applications for microwave frequencies. The optimization includes the scaling of the barrier layer and the gate length as well as parasitic resistance reduction. The DC characterization, S-parameters, and noise analysis of the HEMTs are presented at 300 K and 5 K. In addition, this chapter reports on the noise performance of two broadband cryogenic MMIC LNAs operating at 0.3–14 GHz and 16–28 GHz which implemented the optimized 100 nm gate length InP HEMTs.

2.1 Vertical and lateral scaling

The epitaxial layer structure used in this work (see Fig. 2.1) was grown on $4''$ InP wafers by molecular beam epitaxy. The epitaxial layer was purchased from IntelliEpi. Hall measurements at 300 K without the cap layer exhibited an electron mobility and sheet carrier concentration of 10,850 cm^2/Vs and 3.3×10^{12} cm^{-2}, respectively. The detailed description of the InP HEMT

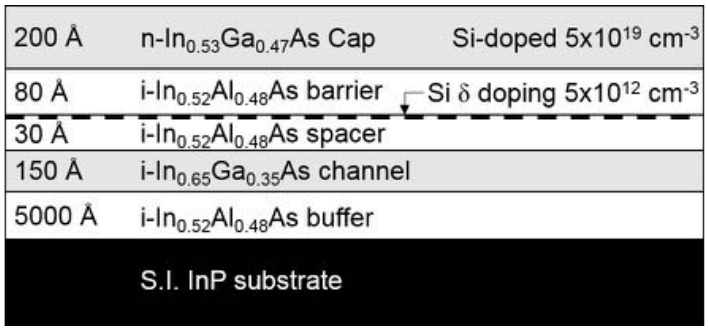


Figure 2.1: The epitaxial layer structure used in this work.

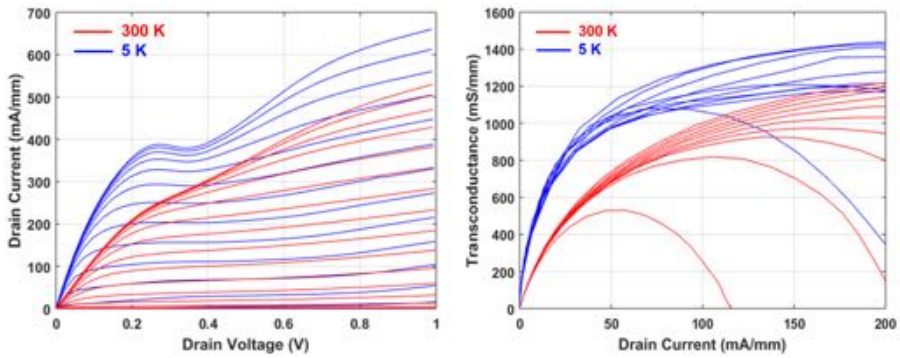


Figure 2.2: I-V characteristics of a 2 × 100 μm gate width and 100 nm gate length InP HEMT. V_{gs} measured from −0.5 V to 0.4 V in steps of 0.04 V (left). Extrinsic transconductance versus drain current density. V_{ds} measured from 0.1 V to 1 V in steps of 0.1 V (right).

fabrication process can be found in Paper [A]. The barrier thickness was 3 nm less than that (11 nm) of our previously reported HEMTs.[10,21] In addition, the gate length was scaled from 130 nm to 100 nm.[10,21] DC and RF measurements of the scaled HEMTs were performed in a LakeShore model CRX-4K cryogenic probe station at 300 and 5 K. Fig. 2.2 shows the output characteristics of a 2 ×100 μm HEMT. The maximum drain current density (I_d) at the drain-source voltage (V_{ds}) of 1 V are 500 mA/mm at 300 K and 650 mA/mm at 5 K. A kink in the drain current for about $V_{ds} = 0.3$ V is observed at 5 K. This is well known electric instability for cryogenic InP HEMTs related to trapping processes occurring at the interfaces and surface of the heterostructure.[22–25] Normally the kink phenomenon is not a problem for a cryogenic LNA since the InP HEMT is biased close to the pinch-off region. However, if the trapping causes memory effects in the HEMT, this may jeopardize reliable cryogenic LNA operation.

The DC transconductance (g_m) as a function of I_d is shown in Fig. 2.2.

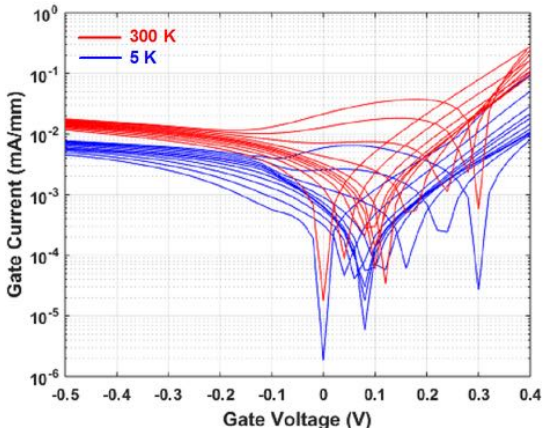


Figure 2.3: Gate current of a 2 × 100 μm gate width and 100 nm gate length InP HEMT at 300 K (red) and 5 K (blue). V_{ds} measured from 0 V to 1 V in steps of 0.1 V.

The slope of g_m at very low I_d is an important indicator of the potential low-noise performance of a device[17] during the DC characterization. In Eq. 2.1, f_T and T_d are strongly dependent on the bias condition. Since f_T and T_d are proportional to g_m and I_d, respectively, the device with higher g_m at low I_d is able to yield low noise performance. At 5 K, g_m reaches 1 S/mm at I_d of only 40 mA/mm which exhibits a steeper increase of g_m compared with the device presented by J. Schleeh *et al.*,[26] where g_m of 1 S/mm was obtained for an higher I_d of 50 mA/mm. The improved slope of g_m can be attributed to improved ratio of the gate length to the gate-to-channel distance.[27,28]

Fig. 2.3 shows the gate current-voltage characteristics at 300 and 5 K. The gate leakage current (I_g) is an critical parameter for the cryogenic LNA noise.[10,17–19] A typical best low-noise gate-source voltage (V_{gs}) for this device is between –0.1 V and 0.1 V and low-noise V_{ds} is approximately 0.5 V. For these voltages, I_g is in the order of 0.1 μA for a 2 × 100 μm HEMT at 5 K. Due to the increase in direct tunneling current with the scaled barrier, I_g is a factor of three higher than the previous work.[21] The impact of this increased I_g on noise performance will be discussed further at the end of this section.

The S-parameter measurements were carried out in a frequency range of 3 GHz to 67 GHz using a Rohde & Schwarz ZVA 67 GHz vector network analyser and GGB Industries' 67A 100 μm pitch wafer probes, both at 300 K and 5 K. The system was calibrated with a GGB CS-5 alumina substrate using a through-reflect-match calibration procedure. Small-signal equivalent circuit parameters at the optimum low-noise bias were obtained using a direct extraction method.[29] A comparison of the equivalent circuit elements from this work and the prior one[21] is presented in Table 2.1. Among the intrinsic parameters, the intrinsic transconductance ($g_{m,i}$) is about 10 % higher than the

Table 2.1: Extracted parameters for the small-signal equivalent circuit of 2×100 μm InP HEMT at the optimum low-noise bias as 300 K and 5 K. Units are V, mA, mS, Ω, fF, pH, and K.

		This work		Ref. 21	
		300 K	5 K	300 K	10 K
Bias	V_{ds}	0.6	0.4	1	0.6
	I_d	16.7	5	15	5
	V_{gs}	-0.02	-0.05	-0.19	-0.16
Intrinsic	C_{gs}	133	139	137	148
	C_{gd}	41	43	31	36
	C_{ds}	84	59	50	51
	$g_{m,i}$	256	244	207	223
	R_i	3.2	0.3	4.1	2.2
	R_j	34	21	36	27
	G_{ds}	16	17	11	14
Extrinsic	C_{pg}, C_{pd}	20	20	8	8
	L_g	6	5	8	10
	L_s	0	0	0	0
	L_d	5	5	8	10
	R_g	1.9	0.6	4	2
	R_d	2.0	0.8	3	2
	R_s	1.8	0.8	2	1

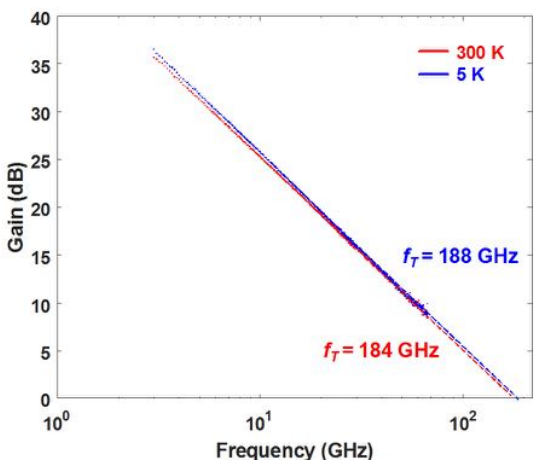


Figure 2.4: Intrinsic current gain $|H_{21}|^2$ of a 2 $\times$ 100 μm gate width and 100 nm gate length InP HEMT at the optimum low-noise bias at 300 K (red) and 5 K (blue).

previously techonology[21] at 5 K. It is also noticed that the extrinsic parameters

Table 2.2: T_g, T_d, I_g, and T_{min} at 6 GHz of a 2×100 μm HEMT, compared with our previous technology. Units are K and μA/mm.

	This work	Ref. 21
T_d	590	630
T_g	4	10
I_g	1.2	0.45
T_{min}	1.2	1.8

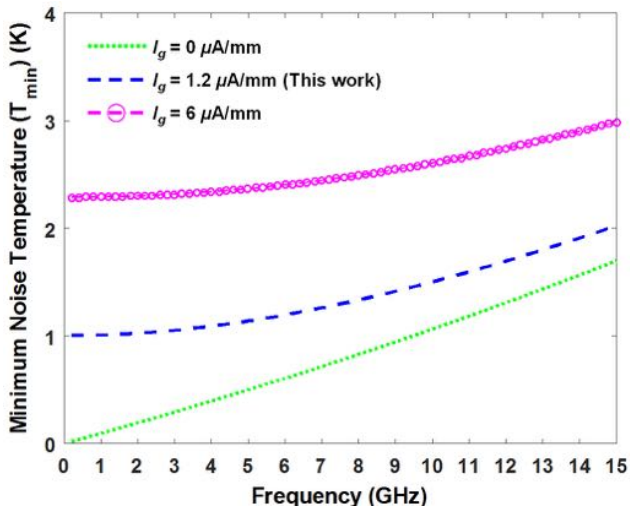


Figure 2.5: Extracted T_{min} of a 2×100 μm InP HEMT exhibiting 1.2 μA/mm gate current (blue dashed) at 4 K compared with the same device without gate current (green dotted) and with 6 μA/mm gate current (magenta dashed with a round) at 4 K.

such as R_g and R_d are improved in this work. The reduction of the parasitic resistance is addressed in section 2.2.

Fig. 2.4 shows the intrinsic current gain $|H_{21}|^2$ against frequency from 3 GHz to 67 GHz at the optimum noise bias. An extrapolated f_T with a slope of –20 dB/dec was 184 GHz at 300 K and 188 GHz at 5 K. Compared to the prior work,[26] the scaled InP HEMT techonology exhibits about 11 % higher f_T at 5 K.

The DC and RF characteristics of the InP HEMT investigated in this work show the potential for cryogenic ultra-low noise performance, in terms of improved $g_{m,i}$ and f_T.

The impact of vertical and lateral scaling of the HEMTs on the noise can be investigated in terms of the minimum noise temperature (T_{min}) of the device. To determine the noise parameters of the HEMTs, the extracted parameters for small-signal model in Table 2.1 were integrated in a AWR Microwave Office

model of the LNA. T_d was extracted by fitting the simulated noise to the measurement of the LNA.[30] I_g was modeled with a shot noise current source using a DC gate current of 1.2 μA/mm measured at the optimum noise bias at cryogenic temperature.[19,31]

Table 2.2 shows T_d, T_g, I_g, and T_{min} obtained from the scaled InP HEMT technology compared to the prior work.[21] The physical temperature was set to be 4 K corresponding to the LNA test ambient (see section 2.3). It is observed that a 0.6 K lower T_{min} at 6 GHz was achieved despite the fact that the 3 nm thinner barrier thickness increased I_g by 60 %. This can be explained in terms of the improvement in $g_{m,i}$ and f_T, whereas I_g does not still dominate the noise.[17,18]

The simulated T_{min} with three different I_g is plotted as a function of frequency in Fig. 2.5. The impact of I_g on T_{min} is much stronger at low frequencies.[17–19] Consequently, a too high I_g will significantly affect the noise performance at a few GHz. The InP HEMT with $I_g = 1.2$ μA/mm has roughly 100 % higher T_{min} (1.2 K) at 6 GHz than the device with $I_g = 0\,\mu$A/mm. In the case of five-fold higher $I_g = 6$ μA/mm, T_{min} of the HEMT increases to 2.4 K (+300 %) which even exceeds the minimum noise temperature ($T_{e,min}$) of the 0.3−14 GHz LNA in this work (see Fig. 2.14). As reported by M. Pospieszalski[17] and J. Shell,[18] when I_g is of the order of 0.1 μA, the device could still yield low-noise performance. In this work, the 2 × 100 μm InP HEMT exhibited I_g of 0.24 μA at the optimum noise bias which is small enough not to dominate the noise performance. However, it is expected that further increase in I_g may significantly deteriorate the noise performance as seen in Fig. 2.5.

2.2 Access resistance reduction

Minimizing the parasitic resistances is another key parameter for reducing the noise contribution of the device[17] as shown in Eq. 2.1. In this work, the source access resistance as well as the gate resistance have been optimized and their impact onto the device as well as noise performance have been investigated.

2.2.1 Source resistance

To improve the ultimate performance of HEMTs, the reduction of R_s plays a central role.[32–34] In order to benefit from high $g_{m,i}$ of the HEMT, R_s should be kept small compared to the inverse of $g_{m,i}$ which in turn yields the noise reduction. R_s is affected by surface states on top of the barrier and by traps between buffer and bottom of the channel.[20,22,35,36] Therefore, scaled barrier in this work will possibly cause increased R_s. In order to reduce R_s, the contact resistance between the ohmic metal and the epitaxial layers (cap, barrier, and channel) should be minimized. This was necessary since the barrier layer was modified in this work. In addition, by decreasing the distance between the gate and the source metal contacts, R_s can be further reduced.

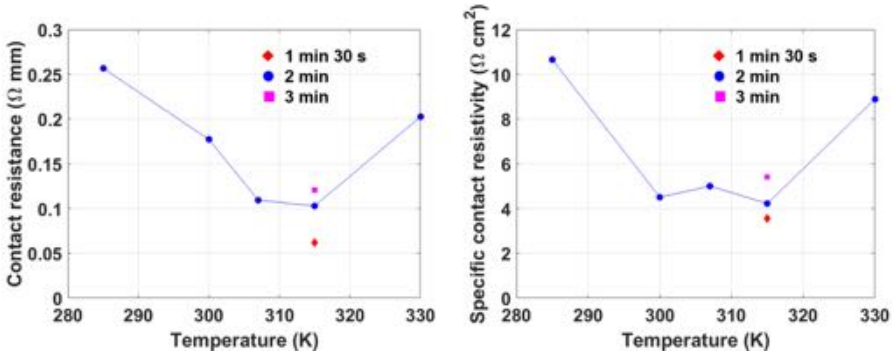


Figure 2.6: Contact resistance measured at 300 K from recessed TLM structures (left) and specific contact resistivity measured from Kelvin structures (right) as a function of annealing temperature.

Ohmic contact resistance

Various combinations as metal stacks in ohmic contacts have been reported.[32, 37–41] In addition to the used metals, the annealing conditions, such as temperature, time, and ambient, have large impact on the contact resistance. In this work, a Ni/Ge/Au ohmic metal stack, which was subject to rapid thermal anneal in an N_2 ambient, was used. During the annealing process, the Ni enhances the reaction between the contact metal and the semiconductor, and the Al in the InAlAs barrier layer out-diffuses to the surface of the contact metal.[37] Then a small fraction of Ge atoms substitutes at these Al sites, resulting in the formation of a Ge-doped n^+-InAlAs layer which increases the carrier tunneling probability, thus reducing the contact resistance.[37] The annealing temperature and time were swept as illustrated in Fig. 2.6 in order to find the optimum condition. The contact resistance was measured from the recessed transfer length method (TLM). In addition, the specific contact resistivity was measured using a Kelvin structure.[42] Fig. 2.6 shows that an optimized ohmic contact was obtained when annealing at 315 °C for 1 min 30 s which resulted in a contact resistance of 0.05 Ω·mm and a specific contact resistivity of $4 \times 10^{-7}\Omega\cdot\text{cm}^2$. The contact resistance measured using the non-recessed TLM (not shown here) resulted in a contact resistance of 0.03 Ω·mm which is comparable to prior work.[10] An extremely low contact resistance of $0.007\,\Omega \cdot$ mm for an InP HEMT was reported by K. Shinohara *et al.*[43] who employed a multilayer cap structure and a non-alloyed ohmic contact. In addition, the non-alloyed contact resistance demonstrates a long-time thermal stability[44] and a nearly temperature independent contact resistance.[41] Hence there is a potential to reduce the present ohmic contact resistance by a factor of 3 to 4 using a more advanced cap layer in combination with non-alloyed contact formation.

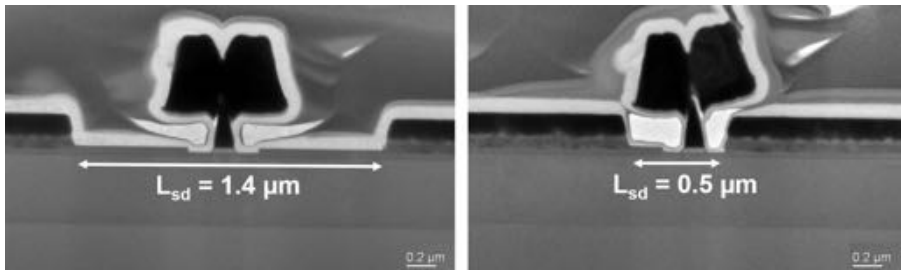


Figure 2.7: Cross sectional STEM image of the InP HEMTs with $L_{sd} = 1.4\,\mu$m (left) and 0.5 μm (right).

Source-drain distance scaling

Along with the ohmic contact optimization, the scaling of the source-drain distance (L_{sd}) was investigated since R_s increases with L_{sd}. The standard L_{sd} in our InP HEMT process has been 1.2 μm. In this work, the HEMTs were designed and fabricated with different L_{sd} varying from 0.6 μm to 1.4 μm, while all other transistor geometries were kept unmodified (Paper [C]). Fig. 2.7 shows cross sectional STEM images of the HEMT with L_{sd} of 1.4 μm and 0.5 μm. In the case of a tight geometry with $L_{sd} = 0.5$ μm, the gate hat is overlapped with the source and drain contacts which increases the parasitic gate capacitance significantly. Moreover, in a process perspective, an inhomogeneous gate resist profile may be formed which will increase the risk of short circuiting the device. Thus only InP HEMTs with $L_{sd} \geq 0.6$ μm were studied in this work.

Fig. 2.8 shows the output characteristics, the maximum drain current ($I_{d,max}$) and maximum transconductance ($g_{m,max}$) at $V_{ds} = 1$ V, and on-resistance (R_{on}) at 300 K. A higher L_{sd} resulted in higher drain current with less pronounced kink phenomena. $I_{d,max}$ was about 800 mA/mm at $L_{sd} = 1.4$ μm at V_{ds} =1 V. This is about 30 % higher $I_{d,max}$ compared to $L_{sd} = 0.6$ μm. In addition, a higher $g_{m,max}$ and lower R_{on} were obtained with increasing L_{sd}.

It is clear from Fig. 2.8 that the scaling of L_{sd} does not yield any improvement in DC performance of the InP HEMT studied in this work. In contrast, I_d and g_m have earlier proven to increase by 25 % when L_{sd} was scaled from 2.3 μm to 1.0 μm for a 130 nm InP HEMT.[45] A possible explanation for the higher $I_{d,max}$, $g_{m,max}$, as well as the lower R_{on} is the traps in the gate recess region occurring for small L_{sd}. This hypothesis is supported by the observation in Fig. 2.8 of a stronger kink effect for smaller L_{sd}. In the case of a large L_{sd}, the lateral electric field in the active region could be too weak to activate surface traps which act to suppress the kink effect.[24] On the other hand, with decreasing L_{sd}, the higher electric field strength activates more surface traps, which in turn resulted in a stronger kink effect in the drain current.

In order to understand the impact of traps on the scaling behavior, the gate recess region was investigated further based on gate cross-sectional analysis

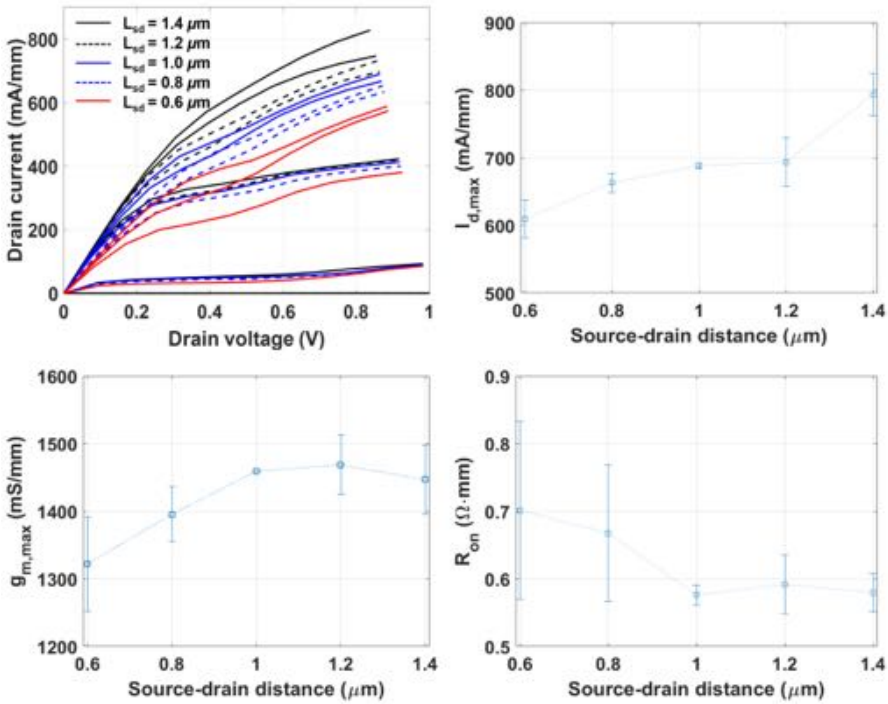


Figure 2.8: The output characteristics of 2×100 μm InP HEMTs at 300 K with L_{sd} ranging from 0.6 μm to 1.4 μm. V_{gs} measured from -0.3 V to 0.7 V in steps of 0.25 V (upper left). The maximum drain current (upper right), maximum transconductance at $V_{ds} = 1$ V (lower left), and on-resistance (lower right) as a function of L_{sd}.

by a scanning transmission electron microscope (STEM). While a wide recess improves breakdown voltage and reduces the feedback capacitance and the gate leakage current, the parasitic source and drain access resistance are increased which reduces the transconductance.[46–48] A typical recess region is shown in Fig. 2.9 (left). During the gate recess etching process, the cap layer was selectively wet etched using succinic acid mixed with H_2O_2 in 4:5 ratio for 40 s and rinsed in water,[49] which gave a 100 nm wide side-recess spacing. It is notable that the InAlAs barrier layer was also etched during recess etching due to the limited selectivity of gate recess wet etching. In addition, the recessed barrier in Fig. 2.9 (left) is not completely flat having dimples at the edges of the gate recessed region. The kink effect highly depends on the recess region as the kink arises from the change in the channel electron density in the recess region.[22,36,51] Therefore, the observation of a non-uniform recess depth as shown in Fig. 2.9 (left) may be one explanation of the strong kink effect and the contradictory scaling behavior of L_{sd} in Fig. 2.8.

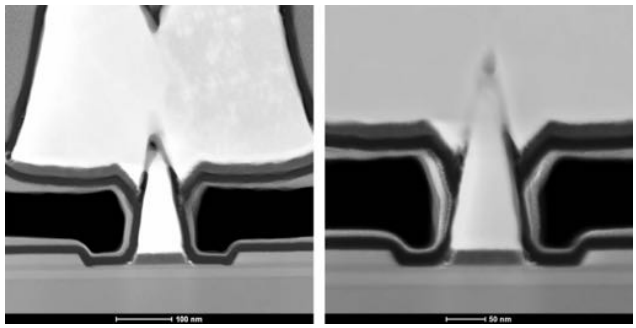


Figure 2.9: STEM images of the gate region without agitation in water (left) and with agitation in water (right) after the gate recess etching.

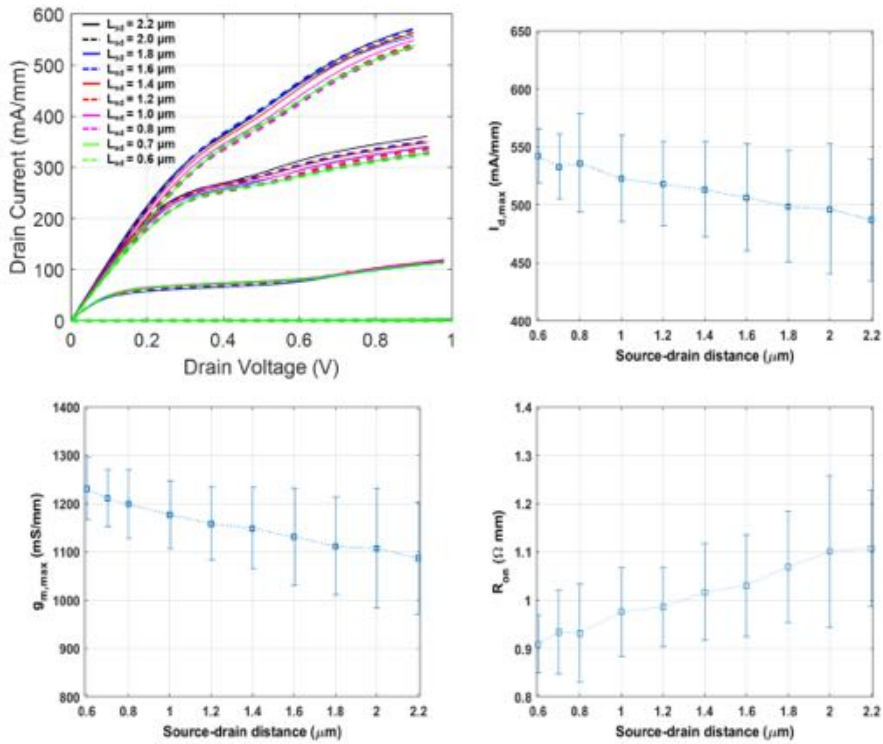


Figure 2.10: The output characteristics of 2×100 μm InP HEMTs at 300 K with L_{sd} ranging from 0.6 μm to 2.2 μm. V_{gs} measured from -0.5 V to 0.4 V in steps of 0.1 V (upper left). The maximum drain current (upper right), maximum transconductance at $V_{ds} = 1$ V (lower left), and on-resistance (lower right) as a function of L_{sd}.

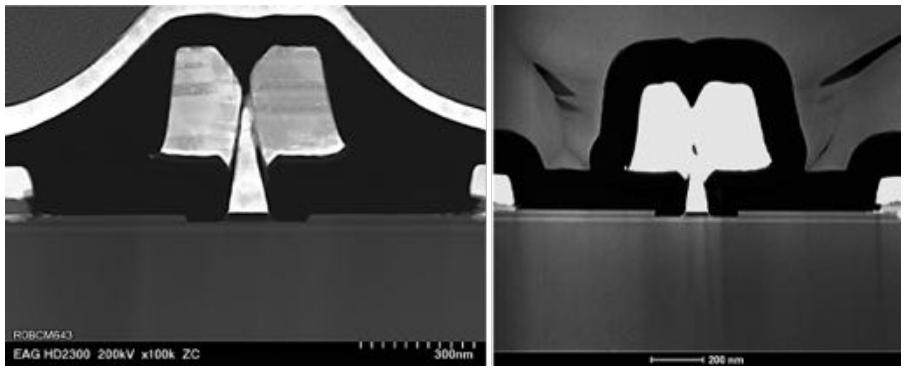


Figure 2.11: Cross sectional STEM image of the InP HEMTs with R_g = 320 Ω/mm[10, 21, 50] (left) and R_g = 230 Ω/mm (right) measured at 300 K.

The dimples at the edges of the recess could be caused by the fact that it takes longer to remove the acid at the far edges since the space where the water has to flow is very tight. Therefore, proper agitation in water, alternatively megasonic cleaning, can help to suppress the non-uniform gate recess etching. In this work, a strong agitation in water after wet etching was tested. In addition, the recess etching time was shorten from 40 s to 30 s in order to explore the impact of the side-recess spacing on L_{sd} scaling. As shown in Fig. 2.9 (right), the recess was 50 nm wide and the dimples at the edges of the recess region disappeared leaving a flat surface in the gate recess. Devices with different L_{sd} ranging from 0.6 μm to 2.2 μm were designed, fabricated, and characterized as can be seen in Fig. 2.10. The kink effect is clearly suppressed in the I−V characteristics which means that less traps seem to be present in these narrow recess regions without dimples. In addition, an increase in $I_{d,max}$ and $g_{m,max}$ and decrease in R_{on} are observed for small L_{sd}. In contrast to Fig. 2.8, the results in Fig. 2.10 are consistent with the scaling of the L_{sd} for the HEMTs published by M. Malmkvist.[45] It is concluded that proper scaling of the InP HEMT can only be done using a uniform gate recess etching where the surface traps are well suppressed.

2.2.2 Gate resistance

With the aim to further minimize the parasitic resistance for the low noise HEMTs, R_g was reduced from 320 Ω/mm to 230 Ω/mm at 300 K, and from 130 Ω/mm to 50 Ω/mm at 5 K.[10, 21] R_g was measured in a gate through-line test structure. Fig. 2.11 compares two gate structures with R_g = 320 Ω/mm (left) and R_g = 230 Ω/mm (right) measured at 300 K. The T-gate fabrication process was optimized by adjusting the electron beam current dose and using a proper resist for a mechanically stable and low resistance gate structure. As a result, Fig. 2.11 (right) shows an improved gate foot and hat connection which resulted in larger mechanical stability as well as a reduced R_g. In addition,

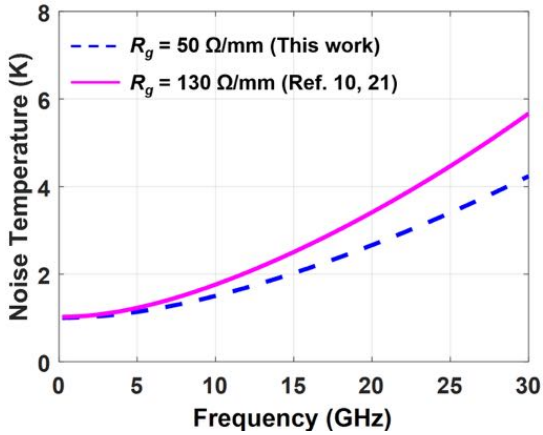


Figure 2.12: Impact of the gate resistance on T_{min} of a 2×100 μm InP HEMT exhibiting $R_g = 50$ Ω/mm (blue dashed) compared with the same device with $R_g = 130\,\Omega$/mm (magenta solid) at 4 K.

about 20 % increase in the gate hat size in Fig. 2.11 (right) also contributed to a reduction in R_g obtained in this work.

In Fig. 2.12, the importance of gate resistance is illustrated by showing two modeled 2×100 μm InP HEMTs either with $R_g = 50$ Ω/mm or with $R_g = 130$ Ω/mm. It should be emphasized that the improvement of the noise temperature due to the reduction in R_g by 60 % at cryogenic temperature is more pronounced at high frequencies above 10 GHz.

2.3 0.3−14 GHz and 16−28 GHz MMIC LNA demonstration

The optimized low noise InP HEMT with 8 nm InAlAs barrier, 100 nm gate length, $L_{sd} = 1.4$ μm, and $R_g = 230$ Ω/mm (at 300 K) were implemented in 0.3−14 GHz and 16−28 GHz MMIC LNAs. The MMICs presented in this work were fabricated before the optimization of gate recess processing. Thus, L_{sd} was designed to be 1.4 μm according to the results shown in Fig. 2.8. The 0.3−14 GHz MMIC LNA was of particular interest since the design was identical to the one using the prior InP HEMT technology.[21] In this way, the impact from the proposed InP HEMT design in this work on the cryogenic LNA performance became visible.

Fig. 2.13 shows photographs of the 0.3−14 GHz and 16−28 GHz LNAs. Both chip sizes are 2 mm × 0.75 mm. The three-stage 0.3−14 GHz GHz LNA uses 2×100 μm transistors and the 16−28 GHz LNA uses 2×50 μm HEMTs. MMIC design details can be found in Paper [B].

The best low noise bias for the 0.3−14 GHz LNA at 300 K was $V_D =$

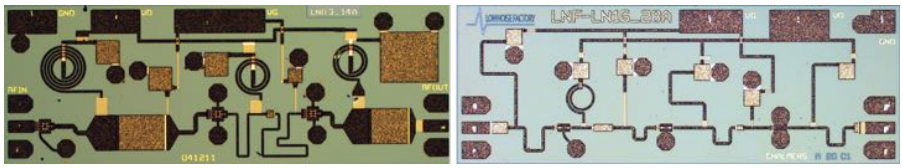


Figure 2.13: MMIC photographs of the 0.3–14 GHz LNA (left) and the 16–28 GHz LNA (right).

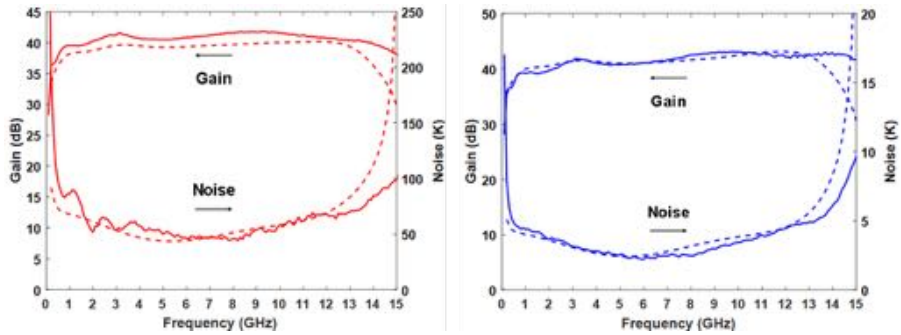


Figure 2.14: Measured (solid line) and simulated (dashed line) gain and noise temperature of the 0.3−14 GHz LNA at 300 K. $V_D = 2$ V, $I_D = 50$ mA (left). Measured (solid line) and simulated (dashed line) gain and noise temperature at 4 K. $V_D = 0.8$ V, $I_D = 15$ mA (right).

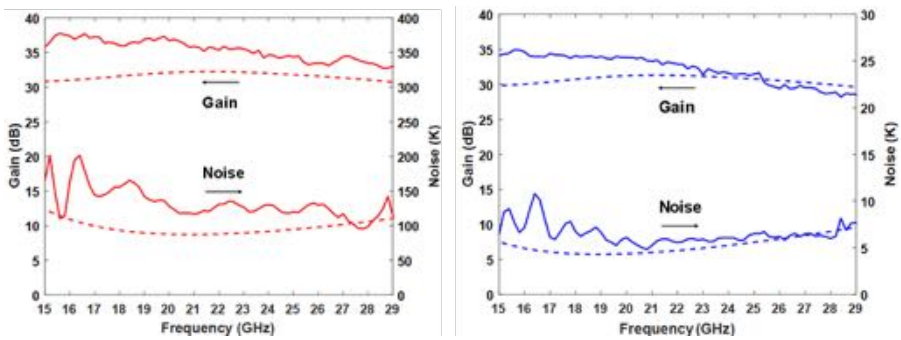


Figure 2.15: Measured (solid line) and simulated (dashed line) gain and noise temperature of the 16−28 GHz LNA at 300 K. $V_D = 1.5$ V, $I_D = 35$ mA (left). Measured (solid line) and simulated (dashed line) gain and noise temperature at 4 K. $V_D = 0.5$ V, $I_D = 7$ mA (right).

2 V and $I_D = 50$ mA. Fig. 2.14 shows the measured and simulated noise temperature and gain at 300 K. The LNA exhibits that the average noise temperature ($T_{e,avg}$) of 60.7 K with $T_{e,min}$ of 44.2 K at 8.2 GHz and 40.7 dB ± 0.9 dB gain.

When cooled down to 4 K, the optimum low noise bias for the LNA was V_D = 0.8 V and I_D = 15 mA. As presented in Fig. 2.14, the amplifier achieved $T_{e,avg}$ of 3.5 K with $T_{e,min}$ of 2.2 K at 6 GHz and 41.6 dB ± 1.4 dB gain.

For the 16−28 GHz MMIC LNA at 300 K, $T_{e,avg}$ was 132.5 K with $T_{e,min}$ of 95.5 K at 27.8 GHz and the gain was 35.5 dB ± 1.3 dB when biased at V_D = 1.5 V and I_D = 35 mA as seen in Fig. 2.15.

At the ambient temperature of 4 K, the LNA was biased at V_D = 0.5 V and I_D = 7 mA and achieved a 32.3 dB ± 1.8 dB gain and $T_{e,avg}$ of 6.3 K with $T_{e,min}$ of 4.8 K at 20.8 GHz.

Table 2.3 displays a comparison of the two LNAs with other published cryogenic wide-bandwidth LNAs for similar frequency ranges.[9,11,21,52–55] The two LNAs presented in this work both exhibited state-of-the-art results in terms of the lowest noise temperature and highest gain per stage with a wide bandwidth at a relatively low power dissipation. Moreover, this was the first demonstration of cryogenic MMIC LNA covering the whole K-band (18 to 27 GHz).

The presented state-of-the-art results were achieved by the optimization of InP HEMTs for cryogenic LNA applications. This can be explained by higher $g_{m,i}$ and f_T as well as parasitic resistance reduction for the InP HEMT. In the case of the 0.3−14 GHz design, a too high I_g would have a large impact on the LNA performance deteriorating the noise significantly.[10,17–19] Despite the three-fold higher I_g due to the scaled barrier, an improved noise temperature was achieved for the 0.3−14 GHz MMIC LNA. In the K-band, both the scaling of the HEMT and reduction in R_g were essential to yield a state-of-the-art cryogenic LNA noise performance.

Table 2.3: Comparison of cryogenic wide-bandwidth LNAs.

Ref.	Process	Type	Freq. (GHz)	Gain (dB)	$T_{e,avg}$@ T_{amb}(K)	P_{dis} (mW)
9	0.1 μm InP HEMT	3-stage MMIC	1-11	33.4±0.3	3.9@4.1	24
21	0.13 μm InP HEMT	3-stage MMIC	0.5-13	38.1	4.4@15	13
52	0.1 μm GaAs mHEMT	3-stage MMIC	4-12	31.5±1.8	5.3@15	8
53	0.1 μm InP HEMT	3-stage MMIC	4-12	37	3.5@12	9.2
54	0.1 μm InP HEMT	3-stage MMIC	4-12	26±1.2	8.1@15	12
This work	0.1 μm InP HEMT	3-stage MMIC	0.3-14	41.6±1.4	3.5@4	12
11	80 nm InP HEMT	-	20-25	-	8@22	-
55	0.1 μm InP HEMT	4-stage Hybrid	20-25	35	27@80	24
This work	0.1 μm InP HEMT	3-stage MMIC	16-28	32.3±1.8	6.3@4	3.5

Chapter 3

InP HEMT design for stable cryogenic operation

The InP HEMT technology has been developed to enable cryogenic LNAs to operate at higher frequencies.[56–60] For high frequencies, LNAs are built on MMICs in which an entire circuit is fabricated on a single chip. Therefore, reliable and reproducible cryogenic LNA operation can only be obtained when a transistor operates in a stable manner at cryogenic temperature.

Abnormal cryogenic HEMT operation has been reported in several studies.[18,60–65] G. Moschetti *et al.*[64] reported that the four-finger metamorphic HEMT (mHEMT) exhibited a hysteretic change in the drain current, and a significant reduction in gain at cryogenic temperature. The observed instability was caused by a resonance induced by an U-shaped drain feeder which connects two drain contacts in the layout of the four-finger transistor. In order to eliminate the resonances, an air-bridge was added across the drain feeder which shifted the resonance frequency toward higher values beyond f_{max} of the mHEMT.

Another solution for stabilization of the cryogenic HEMT operation was proposed by M. Varonen *et al.*[60] The four-finger HEMTs were divided into two discrete two-finger HEMTs. In this way, oscillations at several hundreds of GHz occurring within a four-finger device was avoided. The design technique proposed by M. Varonen *et al.*[60] assumed that the two-finger devices were stable at cryogenic operation. However, instability of the two-finger devices were not yet discussed. This was in fact reported already in 1986.[65] The presence of oscillations at several tens of GHz was noted, but the origin and solution for instabilities were not found. Therefore, cryogenic instability in two-finger InP HEMTs needs to be investigated more in detail. Such device layouts are frequently used in MMIC LNA designs.

In this chapter, the electric stability of two-finger InP HEMTs is investigated at room and cryogenic temperature. Different stabilization solutions are suggested and demonstrated both on device and circuit level by cryogenic measurements.

3.1 Stability characterization

The instability of various gate widths, ranging between 10 μm and 100 μm, and gate lengths, between 60 nm and 130 nm, of two-finger HEMTs at 300 K

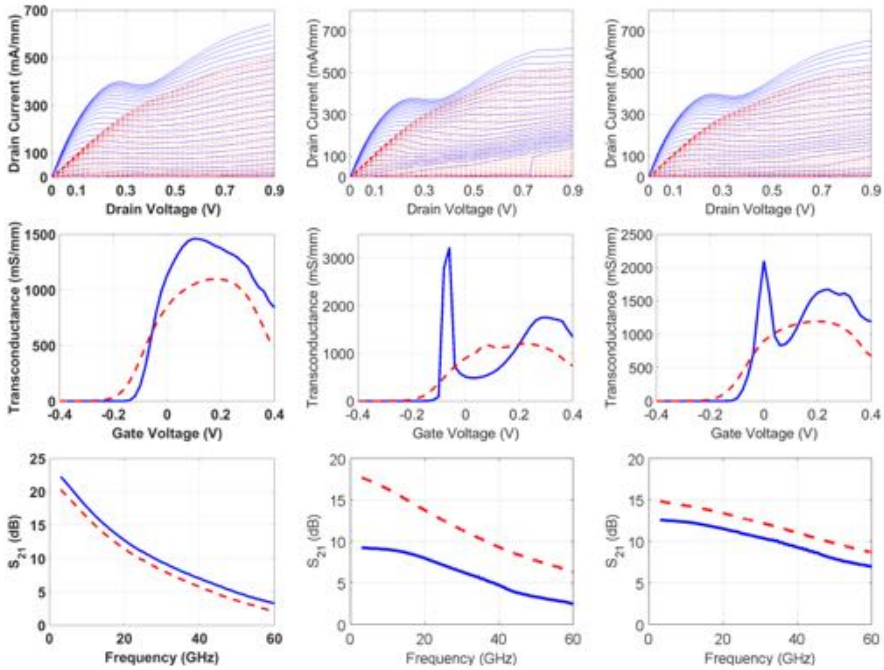


Figure 3.1: The $I-V$ characteristics, transconductance at $V_{ds} = 0.8$ V, and S_{21} at $V_{ds} = 0.8$ V and $J_d = 190$ mA/mm of a 2×100 μm (left column), $2 \times 50\,\mu$m (middle column) and 2×30 μm (right column) 100 nm HEMTs at 300 K (red dashed) and 5 K (blue solid).

and 5 K were investigated. DC measurements were carried out by sweeping the drain voltage in steps of 25 mV for each gate voltage which was in steps of 20 mV. The S-parameter measurements were carried out in a frequency range from 20 MHz to 60 GHz.

Fig. 3.1 presents the I−V characteristics, g_m at $V_{ds} = 0.8$ V and gain (S_{21}) measured at $V_{ds} = 0.8$ V and the drain current density (J_d) = 190 mA/mm at 300 K and 5 K. The measured transistors were 2×100 μm, $2 \times 50\,\mu$m, and 2×30 μm 100 nm gate length HEMTs. The 2×100 μm HEMT shows a continuous drain current and transconductance both at 300 K and 5 K. An increased drain current and gain were also observed at 5 K compared to 300 K which were consistent with the results seen in Fig. 2.2.[18,63]

As the gate width decreases, such as 2×50 μm and 2×30 μm HEMTs in Fig. 3.1, the drain current measured at 5 K suddenly increases with an abrupt step and exhibits a large output conductance not at all observed at 300 K. This gives a drain current region which is not within reach using static bias settings. Moreover, a discontinuous g_m is observed for 2×50 μm and $2 \times 30\,\mu$m HEMTs at 5 K. S_{21} is also significantly decreased by approximately

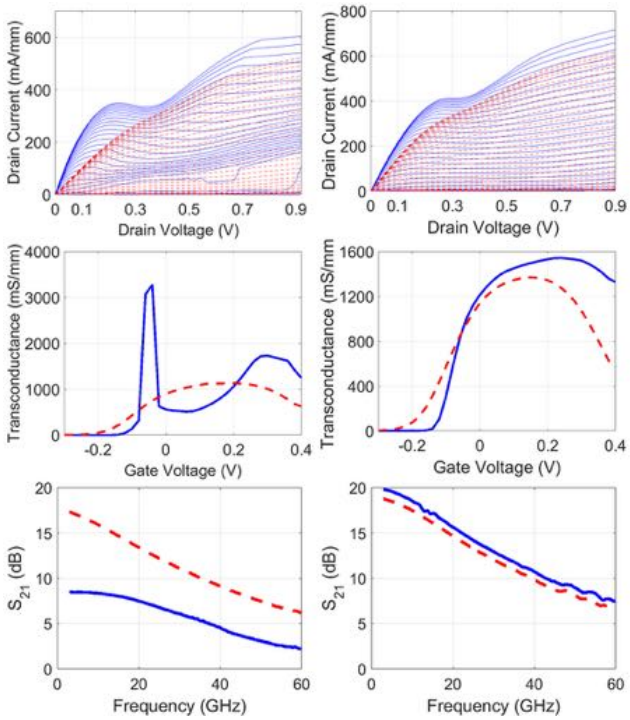


Figure 3.2: The HEMT $I-V$ characteristics, transconductance at $V_{ds} = 0.8$ V, and S_{21} at $V_{ds} = 0.8$ V and $J_d = 190$ mA/mm of a 2×50 μm at 300 K (red dashed) and 5 K (blue solid). The gate length was 60 nm (left column) and 130 nm (right column).

3 to 10 dB at 5 K. However, the observed cryogenic instability disappears for an even smaller gate width, such as 2×10 μm and 2×20 μm HEMTs, which can be found in Paper [A]. It is worth mentioning that the Ka- and Q-band MMIC LNA designs presented below utilize 2×30 μm and 2×50 μm 100 nm gate length HEMTs. Thus, the cryogenic instability observed in Fig. 3.1 must be mitigated for a reliable and reproducible cryogenic LNA performance.

The impact of the gate length on cryogenic instabilities was studied. Fig. 3.2 compares the DC and RF measurement results between two gate lengths, 60 nm and 130 nm. Compared to the 100 nm process (see Fig. 3.1), the 60 nm gate length HEMT exhibits even more unstable behavior at 5 K in terms of a wider inaccessible drain current region and a lower gain. On the other hand, as the gate length increases to 130 nm, the two-finger HEMT shows stable characteristics both at 300 and 5 K similar to the one observed for the 2×100 μm HEMT. The fact that the transistor with a shorter gate length, and thus higher f_{max}, is more unstable, indicates that the instability occurs at high frequencies.[60,64]

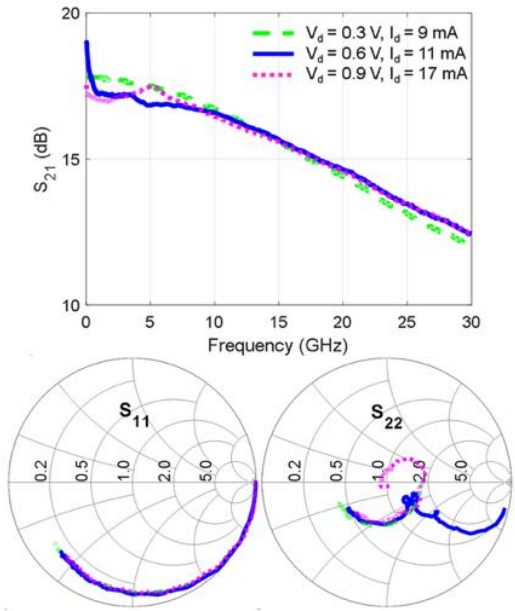


Figure 3.3: The S-parameter measurements of the 2×50 μm device with a 100 nm gate length at V_{ds} = 0.3 V (green dashed), 0.6 V (blue solid), and 0.9 V (magenta dotted). V_{gs} = 0 V at an ambient temperature of 5 K.

It is concluded that anomalous cryogenic behavior for two-finger InP HEMT depends on the device size as well as the gate length. The anomalies appear above a certain device size, 2×20 μm, and disappear at larger gate width, 2×100 μm. The instabilities become more pronounced with a shorter gate length, 60 nm, whereas the investigated DC and RF characteristics for 130 nm InP HEMTs appear stable at 5 K.

The RF cryogenic setup in this study only allowed measurements up to 67 GHz, so it was not possible to experimentally verify the high frequency resonances reported in Ref. 64 to cause the observed device instabilities at cryogenic temperature. Instead, S-parameters were measured in a frequency range from 20 MHz to 67 GHz at 5 K. Fig. 3.3 presents the measured data up to 30 GHz where the abnormal features are observed. The bias point where the drain current suddenly increases is of particular interest. The 2×50 μm 100 nm HEMT is measured at 5 K using V_{ds} = 0.3, 0.6, and 0.9 V, and V_{gs} = 0 V. As seen in Fig. 3.1, the drain current jumps at around V_{ds} = 0.7 V. At a low drain drain bias of V_{ds} = 0.3 V, the S-parameters do not show any indication of instability. However, at V_{ds} = 0.6 V, which is right before the drain current jumps, the S-parameters start to deviate from the standard HEMT model. The S_{21} curve exhibits a spike at a few MHz and fluctuations around 5 GHz. In addition, in the S_{22} trace, an abnormal spike from 20 MHz

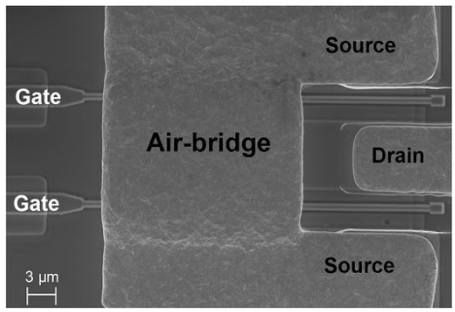


Figure 3.4: SEM image of a two-finger transistor with a source air-bridge.

to 10 GHz is observed. At a higher drain bias of $V_{ds} = 0.9$ V, the transistor oscillates where the drain current and output conductance suddenly increased. As seen in Fig. 3.3, the S_{21} curve fluctuates below 10 GHz at $V_{ds} = 0.9$ V. Fig. 3.3 also shows an inductive shift in S_{22} below 10 GHz which is mainly associated with impact ionization.[66,67] Similar dispersion in S-parameters in the low frequency range, in terms of an abnormal spike and ripples in S_{21}, was reported for four-finger InP HEMTs at cryogenic temperatures.[62] It was claimed that the dispersion observed at low frequencies was related to both the deep level traps in the buffer layer and oscillation.

The small-signal modeling at 300 K and 5 K could provide insight into the mechanism causing the instability. However, extraction of equivalent parameters was not possible; when the device was in the anomalous state, the S-parameters diverged from the standard HEMT model. In addition, the drain current constantly fluctuates for the device in an abnormal state. The mechanism causing the cryogenic instability of two-finger InP HEMTs is not yet clear. Further cryogenic measurements below 20 MHz may give more information regarding the low frequency dispersion as seen in Fig. 3.3 or alternatively by measuring S-parameters at high frequencies (several hundreds of GHz) using a properly designed calibration substrate, potential resonances occurring for the cryogenic two-finger InP HEMT could be proven.

3.2 Design technique

In the layout of a multi-finger transistor, parallel fingers may induce signal mismatch at the edge of the gate.[62] Therefore, odd-mode oscillations may occur due to the inherent asymmetry of the multi-finger transistor.[60,62] The two-finger transistor can be considered as two transistors placed in parallel, partially connected through grounded source contacts. One hypothesis is that the instability may arise when the two devices operate slightly out of phase. The phase difference may occur when two gates are asymmetric due to small variations in the process and from the asymmetry in the parallel source contacts. Thus, a stabilization solution which can make the parallel transistors

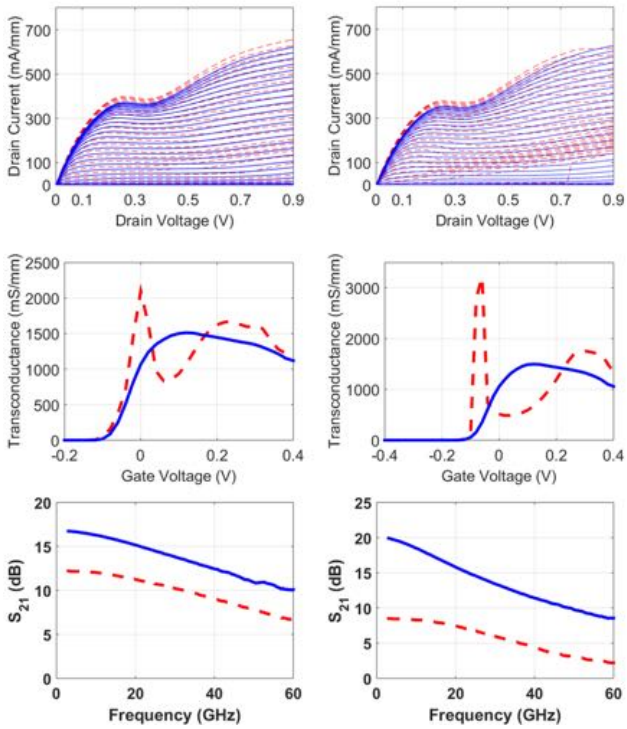


Figure 3.5: The $I-V$ characteristics, transconductance at $V_{ds} = 0.8$ V, and S_{21} at $V_{ds} = 0.8$ V and $J_d = 190$ mA/mm of a 2×30 μm (left column) and 2×50 μm (right column) HEMTs with (blue solid) and without (red dashed) the source air-bridge at 5 K.

to operate in phase should be tested.

In this section, three different InP HEMT designs are presented in order to suppress the observed two-finger 100 nm gate length HEMT instability at 5 K.

3.2.1 Source air-bridge

In order to stabilize the two-finger HEMT, an air-bridge was added across the two source contacts as shown in Fig. 3.4. By connecting the source contacts, the two parallel transistors are expected to have a stronger electric coupling.

Fig. 3.5 compares DC and RF measurements of the 2×30 μm and $2 \times 50\,\mu$m HEMTs with and without the source air-bridge at 5 K. It shows that when adding the source air-bridge, abrupt steps in the drain current and discontinuities in the transconductance curve completely disappear resulting in a largely enhanced S_{21}. These measurements clearly demonstrate that the cryogenic instability in the two-finger HEMT is eliminated with the source air-bridge. The elimination of HEMT instability is probably related to enhanced

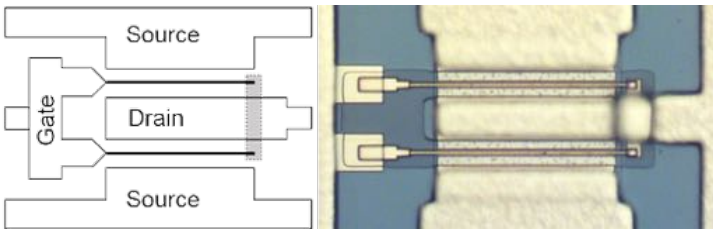


Figure 3.6: Modified layout (left) and micrograph (right) of a two-finger transistor by connecting the back end of the gates.

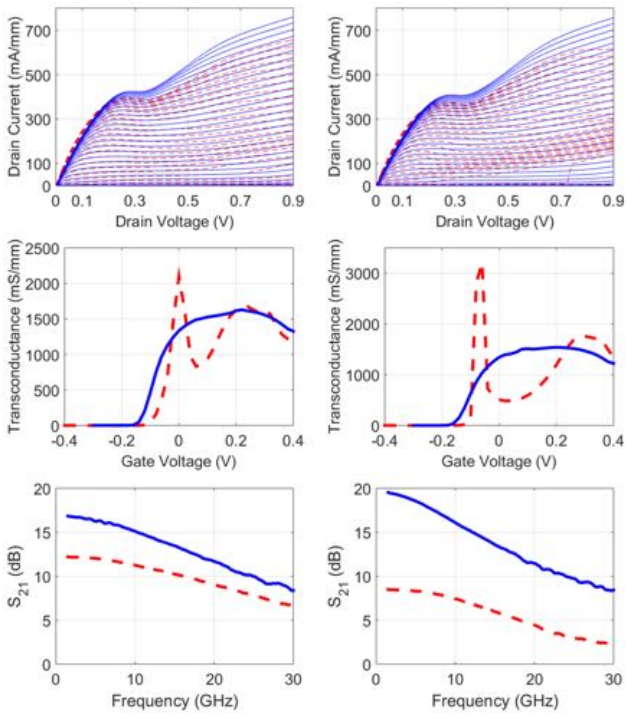


Figure 3.7: The $I-V$ characteristics, transconductance at $V_{ds} = 0.8$ V, and S_{21} at $V_{ds} = 0.8$ V and $J_d = 190$ mA/mm of a 2×30 μm (left column) and 2×50 μm (right column) HEMTs with (blue solid) and without (red dashed) connecting the back end of gates at 5 K.

electric coupling between the two HEMTs.

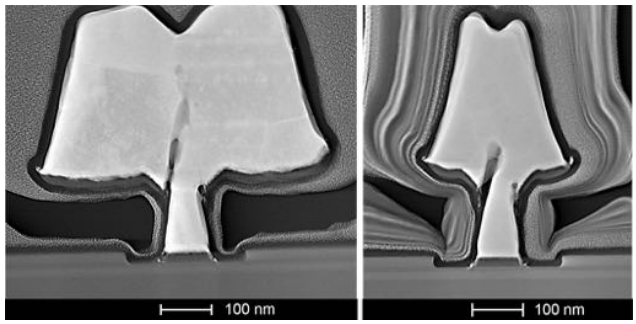


Figure 3.8: Cross-sectional STEM image of the HEMT with a gate resistance of 50 Ω/mm (left) and of 140 Ω/mm (right).

3.2.2 Two gate fingers back end connection

As an alternative way to enhance coupling between the parallel devices, the two gate fingers were connected at their back end with a thin metal strip forming a closed loop. Fig. 3.6 shows the modified layout by connecting the back end of gates. This method allows equalizing the potential at the two gates which in turn force the two parallel transistors to operate in phase.

The 2×30 μm and 2×50 μm HEMTs with and without two gates connected at the back end solution were measured at 5 K and the results are shown in Fig. 3.7. This shows that the devices operated in a stable manner exhibiting the continuous drain current as well as transconductance, and a higher gain at 5 K. These measurements confirm that connecting gates at their back end also strengthens coupling between the two parallel devices which permits stable operation of the two-finger HEMT under cryogenic operation.

3.2.3 Gate resistance modification

As for the third solution, the effect of a gate resistances was investigated. The idea behind this solution was that a higher gate resistance may attenuate potential oscillations within the device, resulting in stable operation of the two-finger InP HEMT at 5 K. In the standard process, the gate resistance was 50 Ω/mm at 5 K which was consistent with the measured value in section 2.2.2. The gate resistance was increased up to 140 Ω/mm by reducing the gate hat size. Fig. 3.8 displays the cross-sectional STEM images of two different gates. Fig. 3.9 demonstrates the impact of the gate resistance on the cryogenic instability of the 2×50 μm HEMT. As the gate resistance is increased from 50 Ω/mm to 90 Ω/mm, the cryogenic instability was suppressed significantly showing a small peak in the transconductance curve only at a high $V_{ds} = 0.8$ V. In the case of the HEMT with a higher gate resistance of 140 Ω/mm, the two-finger HEMT exhibits stable device characteristics regardless of V_{ds}. It confirms that the instability disappears by damping the oscillation by increasing the

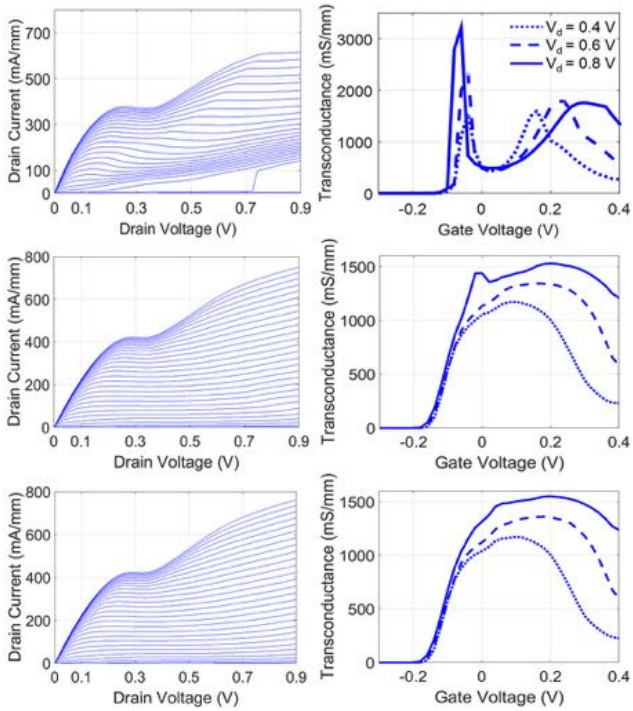


Figure 3.9: The I-V characteristics and transconductance at V_{ds} = 0.4 V (dotted), 0.6 V (dashed), and 0.8 V (solid) of transistors with a 2×50 μm 100 nm HEMT. The gate resistance was 50 Ω/mm (top row), 90 Ω/mm (middle row) and 140 Ω/mm (bottom row) at 5 K.

gate resistance. However, using a higher gate resistance is not a practical solution due to the fact that this solution strongly deteriorates HEMT noise performance.[17] Thus, either adding the source air-bridge or connecting two gates at the back end should be selected in order to effectively stabilize the two-finger devices for a cryogenic LNA.

3.3 24−40 GHz and 28−52 GHz MMIC LNA demonstration

Among two solutions, either adding the source air-bridge or connecting two gates at the back end, a source air-bridge solution is preferred in the MMIC design. This is because the two source contacts are separated through via holes positioned about 50 μm away from the source when the source air-bridge is not present. Thus, the source air-bridge solution is necessary in order to avoid phase variation associated with the long interconnection. In this section,

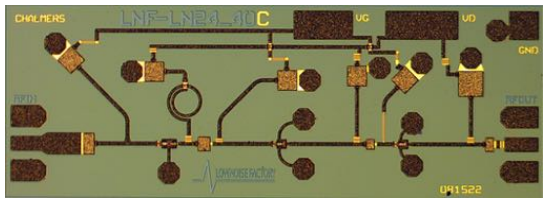


Figure 3.10: A photograph of fabricated three-stage 24–40-GHz MMIC LNA.

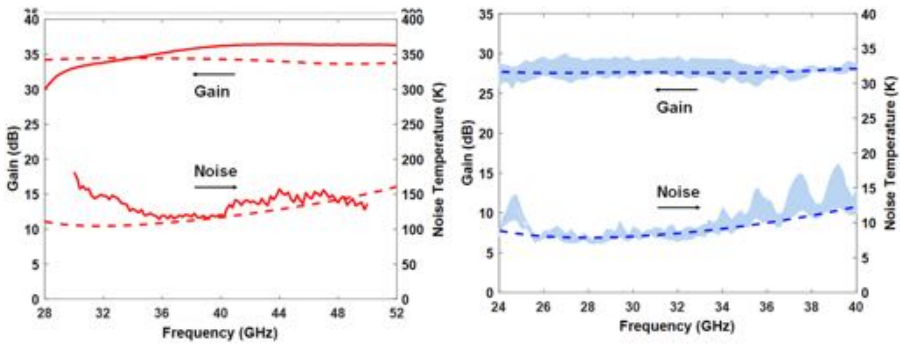


Figure 3.11: Simulated (dashed) and measured (solid) gain and noise temperature of the 24–40 GHz LNA at 300 K. $V_D = 1.2$ V, $I_D = 27$ mA (left). Simulated (dashed line) and measured (solid line and shaded area) gain and noise temperature of eight LNAs at 5.5 K. $V_D = 0.5$ V, $I_D = 5$ mA (right).

the stabilization effect of the source air-bridge technique is demonstrated in three-stage 24–40 GHz (Ka-band) and four-stage 28–52 GHz (Q-band) MMIC LNAs. A photography of Ka-band LNA is presented in Fig. 3.10. The LNA included a 2×50 μm transistor for the first stage, and 2×30 μm transistors for the second and third stage. All transistors utilized the source air-bridge design.

The 24–40 GHz LNA was biased at $V_D = 1.2$ V and $I_D = 27$ mA at 300 K. As seen in Fig. 3.11, $T_{e,avg}$ was 110 K with $T_{e,min}$ of 87 K at 27.6 GHz, and the average measured gain was 31 dB.

When cooled down to 5.5 K, the LNAs were measured at the optimum noise bias of $V_D = 0.5$ V and $I_D = 5$ mA. Fig. 3.11 shows the measured and simulated noise temperature and gain of eight LNA chips. The LNAs exhibited $T_{e,avg}$ of 10.6 K with $T_{e,min}$ of 7 K at 25.6 GHz and the average measured gain of 29 dB. It also demonstrated the excellent uniformity of the LNA design with the source air-bridge solution along the wafer.

Two version of the MMIC LNA design in the Ka-band was fabricated: one with and one without the source air bridge for each transistor. This made it possible to see the importance of HEMT stability at cryogenic operation. Fig. 3.12 compares the measured noise temperature and gain between two

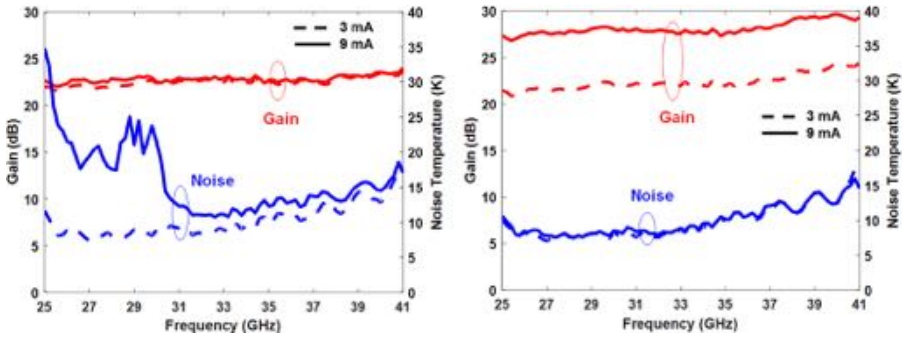


Figure 3.12: Measured gain and noise temperature of the MMIC LNA without (left) and with (right) the source air-bridge operating at 24–40 GHz at an ambient temperature of 5.5 K. $V_D = 1$ V, $I_D = 3$ mA (dashed) and 9 mA (solid).

variants at 5.5 K. The noise temperature for the LNAs was measured using a cold attenuator setup with a maximum uncertainty of less than 1.3 K.[68] The MMIC LNA with the non-stabilized HEMTs in Fig. 3.12 (left) exhibited a drastic increase in the noise temperature as the drain current changed a small amount from 3 mA to 9 mA while the gain stayed at the same value of about 22 dB.

The 24–40 GHz LNA with the source air-bridge design was tested at the same bias conditions as shown in Fig. 3.12 (right). When the drain current increased from 3 mA to 9 mA, the noise temperature unchanged whereas only the gain increased from 22 dB to about 28 dB. The measurements in Fig. 3.12 clearly demonstrate the stabilization effect of the source air-bridge technique at the circuit level at cryogenic temperature.

The stabilization effect of the source air-bridge was also demonstrated in a four-stage 28–52 GHz MMIC LNA which presented $T_{e,avg}$ of 10 K with $T_{e,min}$ of 6.7 K at 32.8 GHz and the average gain of 34 dB at an ambient temperature of 5.5 K. Detailed circuit schematic, photo and LNA results at 300 K and 5.5 K can be found in Paper [A].

Table 3.1 compares the performance of the cryogenic HEMT MMIC LNAs of this work with previously reported LNAs, operating in similar frequency ranges and ambient temperatures.[12,13,21,52,69–71] The two cryogenic MMIC LNA design presented in this work both exhibit state-of-the-art performance in terms of the noise temperature, bandwidth as well as gain. These cryogenic MMIC LNA data confirm the potential of the proposed InP HEMT design and the two-finger HEMT stability solution using the source air-bridge described in Chapter 2 and 3, respectively.

Table 3.1: State-of-the-art cryogenic Ka- and Q-band LNAs.

Ref.	Process	Freq. (GHz)	$T_{e,min}$	$T_{e,avg}$@T_{amb}(K)	Gain/Stage (dB)
12	0.1 μm InP HEMT	26-40	9.3	11.4@12	7.2
21	0.13 μm InP HEMT	24-40	10	13.2@15	9.3
52	0.1 μm GaAs mHEMT	25-34	-	15.2@15	8.1
69	80 nm InP HEMT	26-40	8	12.5@15	9
This work	0.1 μm InP HEMT	24-40	7	10.6@5.5	9.7
13	60 nm InP HEMT	35-50	-	13@20	7
70	70 nm GaAs mHEMT	33-50	13.5	18.4@15	6.8
71	0.1 μm InP HEMT	40-45	-	15@18	8.6
This work	0.1 μm InP HEMT	28-52	6.7	10@5.5	8.5

Chapter 4

Conclusions and future work

4.1 Conclusions

This thesis has demonstrated scaling and stability solutions for a 100 nm gate length InP HEMT technology intended for cryogenic LNAs up to 50 GHz.

By scaling the gate length and barrier thickness combined with reduction of source and gate resistances, advances in cryogenic noise performance for wide-band MMIC LNA were demonstrated in the frequency range of 0.3−14 GHz and 16−28 GHz despite a three-fold increase in the gate leakage current. A study on the source-drain distance scaling revealed that the presence of surface defects strongly affected the electric device performance of the HEMTs also at 300 K. This implied the importance of a careful gate recess etching in the InP HEMT.

Cryogenic stability of two-finger InP HEMTs has been investigated. Unstable cryogenic behavior in terms of jumps in drain current, discontinuous peaks in transconductance, and low-frequency dispersion in the S-parameters were observed. The instability was associated with the partial connection between the two parallel transistors. Stabilization solutions which made the parallel transistors to operate in phase were presented. By either adding a source air-bridge or connecting the back end of the gates, the device instability at cryogenic temperature was eliminated due to enhanced electric coupling between the two HEMTs. The instability was also suppressed by increasing the gate resistance which damped the oscillation. The source air-bridge solution was implemented in two wide-band cryogenic MMIC LNA designs in the frequency range of 24−40 GHz and 28−52 GHz demonstrating state-of-the-art noise performance.

4.2 Future work

The surface traps should be suppressed since the electric device performance of the HEMTs was strongly affected even at 300 K. Therefore, a selective recess etching of the cap to the barrier needs to be improved in order to achieve more reliable and reproducible InP HEMT technology. As introduced by Enoki *et al.*,[72,73] the InP etch stop layer on top of the InAlAs barrier layer will protect the aluminum containing barrier layer against oxidation. The InP etch stop layer also suppresses the kink effect by passivating defects in the recess region

adjacent to the gate.[23] The impact of the InP etch stopper on cryogenic LNA noise performance needs to be performed.

In addition, the development of non-alloyed ohmic contacts will give better control in the processing, a temperature-independent contact resistance, and a long-time thermal stability.[41,44] Combined with an advanced multilayer cap structure as reported by Shinohara *et al.*,[43] the contact resistance can be reduced.

The origin of the cryogenic instabilities in two-finger HEMTs needs to be better understood. Cryogenic measurements below 20 MHz may give more information regarding the low frequency dispersion as seen in section 3.1, or alternatively by measuring S-parameters at high frequencies (several hundreds of GHz) using a properly designed calibration substrate, potential resonances occurring for the cryogenic two-finger InP HEMT could be proven.

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Acknowledgements

I would like to thank my supervisor Jan Grahn, for his support, help, feedback, and encouragement. I would also like to thank my examiner Jan Stake for his guidance in my graduate studies.

I would also like to extend my sincere gratitude to my co-supervisors Per-Åke Nilsson and Giuseppe Moschetti for a lot of constructive discussions, training, suggestions, feedback and support.

Moreover, I would like to give special thank to Niklas Wadefalk and Joel Schleeh for fruitful discussions, LNA design and measurements, and for their enthusiastic collaboration.

I want to thank Arsalan Pourkabirian for helping me to integrate in the group, for the training for device fabrication and measurement, and for many nice discussions.

I would like to show my appreciation to: Stella Bevilacqua (for helping with on-wafer calibration and RF measurements); Piotr Starski (for meaningful discussions and his insight); Hannes Hanhineva (for LNA measurements); Bengt Nilsson, Göran Alestig, John Halonen and NFL people (for advise and assistance in processing); and Silvia Tuzi (for STEM images).

Big thanks go to all my colleagues at MEL and TML. It is truly a pleasure to work among such excellent colleagues.

I would like to end by giving my deepest appreciation to all my friends and my family in Korea.