E-mode Planar $L_g = 35$ nm In$_{0.7}$Ga$_{0.3}$As MOSFETs with InP/Al$_2$O$_3$/HfO$_2$ (EOT = 0.8 nm) Composite Insulator

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Abstract

We have successfully demonstrated a three-step recess process to fabricate high performance E-mode planar InGaAs MOSFETs. Our devices feature a composite gate insulator with InP/Al$_2$O$_3$/HfO$_2$. An $L_g = 35$ nm InGaAs MOSFET with EOT = ~ 0.8 nm exhibits $V_{th} = 0.17$ V, $R_{ON} = 285$ Ohm-$\mu$m, DIBL = 135 mV/V and $S = 115$ mV/dec, as well as a negligible dispersion and hysteresis behavior. Most importantly, our device displays the highest value of $g_{m, max}$ > 2 mS/$\mu$m at $V_{DS} = 0.5$ V in any III-V MOSFETs.

Introduction

The outstanding carrier transport properties of III-V compound semiconductors have fueled interest on these materials for use in the channel material of a future scaled CMOS technology [1-9]. Particularly, indium-rich In$_x$Ga$_{1-x}$As ($x > 0.53$) materials are endowed with very high electron mobility ($\mu_{enh}$) and virtual-source-injection velocity ($v_{as}$). Not only are both quantities directly related to the FET theory and carrier transport properties, but also unique device FOM that ultimately determines the drain current density (I$_{ON}$) and the transistor switching speed (CV/I).

In this paper, we propose a three-step recess process that allows us to fabricate high performance enhancement-mode (E-mode) planar InGaAs MOSFETs with InP/Al$_2$O$_3$/HfO$_2$ composite insulator. Our long- and short-channel MOSFETs with EOT = ~ 0.8 nm exhibit excellent carrier transport properties and logic characteristics.

Experimental

Fig. 1 shows a cross section of the device. From top to bottom, the epitaxial layer structure consists of a heavily doped multi-layer cap (In$_{0.7}$Ga$_{0.3}$As, In$_{0.53}$Ga$_{0.47}$As, InP, In$_{0.52}$Al$_{0.48}$As), 1-nm InP insulator, 10-nm In$_{0.5}$Ga$_{0.47}$As channel, 5-nm In$_{0.52}$Al$_{0.48}$As spacer, inverted Si $\delta$-doping, and 300-nm In$_{0.52}$Al$_{0.48}$As barrier on InP substrate. We have optimized a growth temperature and inverted Si $\delta$-doping density which led to the electron Hall mobility ($\mu_{enh}$) close to $8,500$ cm$^2$/V-sec with $n_{enh} = 1 \times 10^{22}$ cm$^{-2}$ at 300 K. Fig. 1, shows conduction-band (E$_C$) and carrier concentration ($n_x$) profile at S/D access region. Black-colored lines are with n$^+$ In$_{0.53}$Ga$_{0.47}$As cap, whereas blue-colored ones with n$^+$ In$_{0.52}$Al$_{0.48}$As cap. Not only does a use of heavily doped In$_{0.52}$Al$_{0.48}$As cap lower a potential barrier through both InP layers in the S/D access region, but it also significantly increases the electron concentration in the channel. Both are very effective in reducing $R_S$ and $R_D$.

Fig. 1 (Left) Schematic of recessed planar InGaAs Quantum-Well (QW) MOSFETs with InP/Al$_2$O$_3$/HfO$_2$, and (b) (Right) 1D simulation at S/D access region (A-to-B).

Fig. 2 highlights a proposed three-step gate process in this work. After S/D ohmic contact with 2 $\mu$m spacing, a fine gate pattern using single-layer ZEP-520A is defined by e-beam lithography. This is transferred to a passivating SiO$_2$ layer by CF$_4$ plasma (a). Following this, InGaAs cap is etched isotropically using a mixture of citric acid and H$_2$O$_2$, and the InP cap and part of the InAlAs cap are etched anisotropically by a low-damage Ar-plasma (b). Remaining In$_{0.52}$Al$_{0.48}$As cap is fully etched by using a diluted citric acid solution (c). Immediately after removing the ZEP520A, Al$_2$O$_3$/HfO$_2$ (0.5/1.5 nm) is sequentially deposited at 250 $^\circ$C by ALD (d). Finally, a gate metal stack of Pd/Ti/Au is formed.

Fig. 3 shows a SEM image after three-step recess, and a TEM image for the cross section of a 35-nm device. In addition to the e-beam defined narrow gates, we have made optical gate patterns from 4 $\mu$m to 1 $\mu$m, to investigate a carrier transport property.

Fig. 2 Sketch of proposed three step gate recess process.

(a) Selective wet etch
(b) Ar-based RIE
(c) Slow wet etching
(d) Al$_2$O$_3$/HfO$_2$ by ALD.
Fig. 3 (Left) SEM image after three-step-recess. This corresponds to the step (c) in Fig. 2. Final opening by slow wet etching for n+ InAlAs cap determines the physical gate length (Lg). (Right) TEM image for Lg = 35 nm In0.7Ga0.3As MOSFETs with InP/Al2O3/HfO2 composite insulator. Gate metal is made out of Pd/Ti/Au stack.

Results and discussion

A. Long-channel InGaAs MOSFETs

Fig. 4 shows subthreshold and gate leakage current (I_G) of Lg = 2 μm (optical) devices with Mo/Ti/Pt/Au gate metal stack for two types of gate insulators, such as HfO2 (black) and Al2O3/HfO2 (red). Using ~0.5 nm Al2O3 as an ICL (Interface-Control-Layer) [6] leads to a far better interface quality on MBE-grown 1-nm InP, clearly manifested in the subthreshold behavior, such as DIBL = 40 mV/V. We have carried out a pulsed I-V measurement, to evaluate the dielectric-to-channel interface quality, as shown in Fig. 5. Pulse width is 200 ns, and operating condition (bias point) is VGS = -0.8 V and VDS = 1 V in dynamic I-V measurement. Consistent with subthreshold characteristics, the device with composite Al2O3/HfO2 insulator exhibits almost a dispersion-free behavior, in comparison to one with HfO2 insulator.

Fig. 6 shows transconductance (gm) characteristics of various Lg (optical) devices with Mo/Ti/Pt/Au metal gate on Al2O3/HfO2 insulator at VDS = 1 V.

In trying to understand such performance, we have carried out a carrier transport analysis in the sense of ‘effective’ mobility (μ_eff), somewhat similar to [10]. At VDS = -0 V, we first measured high-frequency small-signal S-parameters up to 50 GHz, and then performed a small-signal modeling to extract total gate capacitance (Cg,total = Cgs + Cgd) for various different values of Lg, with Rs and Rd removed. The intrinsic gate capacitance (Cgi) and intrinsic charge (Qgi) are extracted by using the same procedure in [10], and were plotted in the inset of Fig. 7. Finally, μ_eff was computed based on Qgi and goi, and plotted in Fig. 8. Interestingly, the mobility flattens out for low ns. This is an area where the traditional technique fails because of Dit contamination, whereas the proposed technique doesn’t suffer from both capacitance and conductance are extracted from high-frequency S-parameters. At ns = 2 × 10^{12} /cm^2, a long channel device exhibits μ_eff in excess of 7,000 cm^2/V-s.
B. Short-channel InGaAs MOSFETs

Fig. 9 shows typical output characteristics of $L_g = 35$ nm In$_{0.7}$Ga$_{0.3}$As MOSFET with Pd/Ti/Au metal gate on composite Al$_{2}$O$_{3}$/HfO$_{2}$ insulator. Particularly, Pd was chosen for E-mode operations due to its higher work-function. The device exhibits excellent pinchoff and saturation behavior up to $V_{DS} = 0.5$ V. A fairly low value of $R_{ON} = 285\ \Omega \cdot \mu m$ is obtained.

Fig. 10 shows subthreshold and transfer characteristics of $L_g = 35$ nm In$_{0.7}$Ga$_{0.3}$As MOSFET with Pd/Ti/Au metal gate on composite Al$_{2}$O$_{3}$/HfO$_{2}$ insulator. Using a criteria of $I_D = 1\ \mu A/\mu m$, the device shows as follows: $V_T = +0.17$ V (E-mode), $S = 115$ mV/dec and DIBL = 135 mV/V. Besides, our device exhibits very little hysteresis behavior of less than 10 mV.

C. Benchmarking and Discussion

In order to assess the significance of our work, we have benchmarked our devices against reported III-V MOSFETs. Fig. 12 compares $g_{m_{\text{max}}}$ versus $L_g$ of our recessed In$_{0.7}$Ga$_{0.3}$As MOSFETs to prior reports on III-V MOSFETs in the literature. Clearly, the devices in this work exhibit the highest $g_{m_{\text{max}}}$ from long channel to sub-100 nm regime of all the III-V MOSFETs.

Fig. 13 compares $Q$-factor of our recessed In$_{0.7}$Ga$_{0.3}$As MOSFETs with composite Al$_{2}$O$_{3}$/HfO$_{2}$ insulator to other reports, as proposed in [11]. The result in this work indicates $Q = 20$, which is the highest in any III-V MOSFET. Fig. 14 plots virtual-source injection velocity ($v_{x0}$) against DIBL for InGaAs MOSFETs at $V_{ds} = 0.5$ V, together with those of III-V HFETs and Si nFETs [10]. As in [10], $v_{x0}$ increases as DIBL increases. At $V_{ds} = 0.5$ V and DIBL = 100 mV/V, $v_{x0}$ in our InGaAs MOSFETs is about 6x higher than that of state-of-the-art strained Si MOSFETs.
exhibit the highest value of $g_{m_{\text{max}}}$ in any III-V MOSFETs at $S = 115 \text{ mV/dec}$. Most importantly, our device exhibits 7,000 cm$^2$/V-s at $n_s = 2 \times 10^{12}/\text{cm}^2$ at room temperature.

A striking aspect of our In$_{0.7}$Ga$_{0.3}$As MOSFETs with composite insulator (InP/Al$_2$O$_3$/HfO$_2 = 1/0.5/1.5$ nm) is their excellent transport and logic characteristics at $V_{DS} = 0.5$ V, together with aggressive EOT scaling ($\text{EOT} = ~0.8$ nm). Finally, Fig. 15 summarizes the on-resistance ($R_{\text{ON}}$) as a function of $L_g$ for In$_{0.7}$Ga$_{0.3}$As MOSFETs in this work. Inset is a sketch that describes each portion of source-resistance ($R_s$), such as $R_c$, $R_{\text{acc}}$, $R_{\text{Barrier}}$ and $R_{\text{side}}$. Upper inset highlights extracted values for each component in $R_s$.

**Acknowledgment**

This work was supported by the internal R&D program at Teledyne Scientific Company (TSC). The authors would like to thank Eric Regan at TSC for help with the device fabrication, and Prof. Jesus del Alamo and Prof. Dimitri Antoniadis at MIT for fruitful technical discussion and advise.

### Summary

We have demonstrated E-mode planar $L_g = 35$ nm InGaAs MOSFET with composite InP/Al$_2$O$_3$/HfO$_2$ insulator, based on three-step recess process. $L_g = 35$ nm devices exhibit excellent transport and logic characteristics at $V_{DS} = 0.5$ V, such as $g_{m_{\text{max}}} = 2.1 \text{ mS/\mu m}$, $R_{\text{ON}} = 285 \Omega/\mu m$. DIBL is 135 mV/V and $S = 115$ mV/dec. Most importantly, our device exhibits the highest value of $g_{m_{\text{max}}}$ in any III-V MOSFETs from long channel to sub-100 nm regime. In addition, we have carried out a carrier transport analysis, indicating $\mu_{\text{eff}} > 7,000 \text{ cm}^2/\text{V-s}$ at $n_s = 2 \times 10^{12}/\text{cm}^2$ at room temperature.

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